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SYNTHESIS OF PETRI NETS USING LATCHES CIRCUITS

Mihai Timis
Universitatea Tehnica "Gh. Asachi" Iasi
Facultatea de Automatica si Calculatoare
Catedra Calculatoare
mtimis@cs.tuiasi.ro

Abstract - In this paper, the author proposes a synthesis method of Petri Nets using latches circuits. Using a Petri Net graph, will be deducted the input and output matrix values. These values will represent the inputs respectively the outputs of the latches circuits. It can be observed that the entire system will be design as an asynchronous sequential circuit using latches circuits (Flip Flops). These circuits has no clock input signal, so the entire digital system will be asynchronous, with no clock. It will transit on to next state only when new inputs signals are changed. The method presents how can be reduced the synthesis of asynchronous digital systems from Petri Nets graphs to latches - flip flop circuits design.

Keywords: J-K latch, flip flop, asynchronous sequential system design, Petri nets, logic gate, input, output matrix.

I. INTRODUCTION

The Petri nets networks are represented by graphs. It is said that a graph is completely defined if there are known all his nodes and arcs, figure 1.

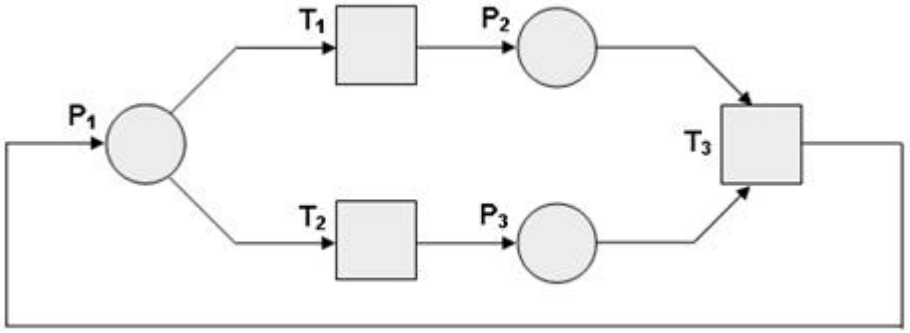

Figure 1

The Petri network is composed by C=(P,T,I,O) where $p_i \in P, i = 1...N$ represents the processes, $t_j \in T, j = 1...L$ the transitions, I and O input – output matrix. These matrix represents the description of the input – output transitions from the processes on Petri network. Every line from the matrix represent a transition, every column represent a processes. The links between them represents a weight, W. If there is a connection W=1, if no, W=0.

Petri nets are used to design different digital systems. For a good design, the Petri network must be safe – states cycles not allowed.

II. METHOD DESCRIPTION

The network is safe, so we will assign on every process a latch circuit. On every transition t_i will be assigned an event e_i. It is also possible to assign on every transition a state s_i. Let's consider the Petri nets graph described like in figure 2.

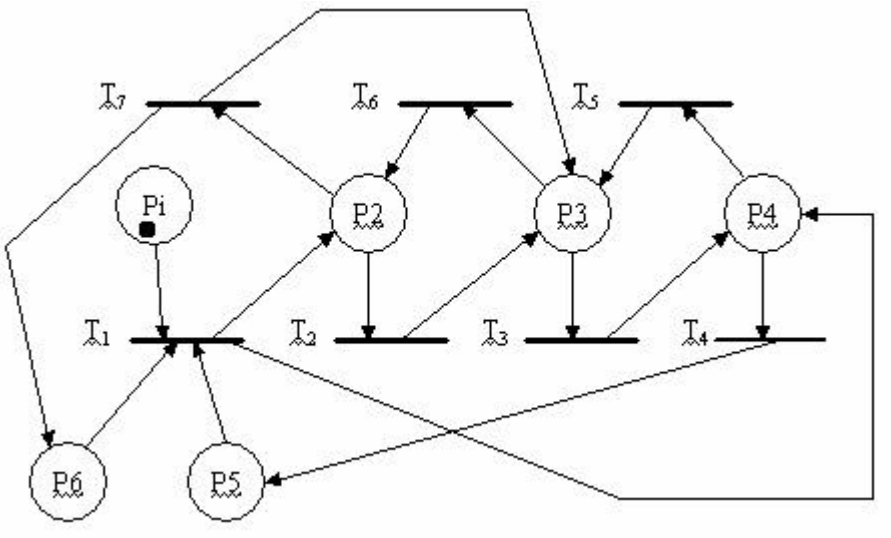

Figure 2

The Petri nets graph from figure 2 consists of 7 processes – states (P) and 7 transitions (T).

- on transition T_1 enters P_1, P_6 and P_5 processes and out P_2 and P_4 processes.
- on transition T_2 enters P_2 and out P_3.
- on transition T_3 enters P_3 and out P_4.
- on transition T_4 enters P_4 and out P_5.
- on transition T_5 enters P_4 and out P_3.
- on transition T_6 enters P_3 and out P_2.
- on transition T_7 enters P_2 and out P_3 and P_6.

Using figure 2 we will make the input matrix and output matrix for the Petri net system, (1).

$$I = \begin{matrix} 1 & 0 & 0 & 0 & 1 & 1 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 \end{matrix} \quad (1)$$

$$O=\begin{matrix}0&1&0&1&0&0&0\\0&0&1&0&0&0&0\\0&0&0&1&0&0&0\\0&0&0&0&1&0&0\\0&0&1&0&0&0&0\\0&1&0&0&0&0&0\\0&0&1&0&0&1&0\end{matrix}$$

$$I+O=\begin{matrix}1&1&0&1&1&1&0\\0&1&1&0&0&0&0\\0&0&1&1&0&0&0\\0&0&1&0&1&0&0\\0&0&1&1&0&0&0\\0&1&1&0&0&0&0\\0&1&1&0&0&1&0\end{matrix}$$

Next, these matrix will be used to design the asynchronous sequential system with latches circuits. Every “i” column is connected to out Q of the J-K latch, every t_i line represent the transitions performed by the system. When a transition is done, the marked point associated with it will be deleted. When a marked point is assigned on system, the J-K latch is on the first state, 1. When the marked point is deleted from the system, the J-K latch is on the second state, 0, figure 3.

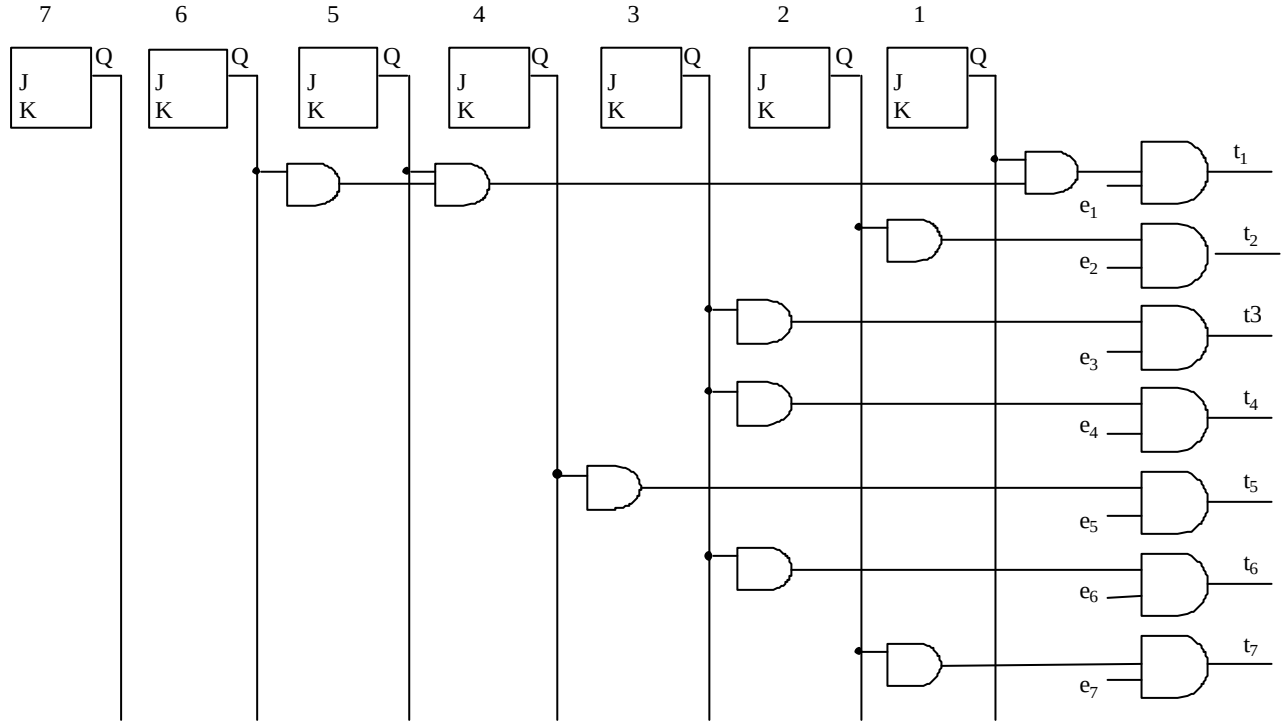

Figure 3

The J-K inputs of the latch circuit has the same wire, when a 1 logic value is present, the latch change it value, transit to next state. The latch design during transitions is described on figure 4.

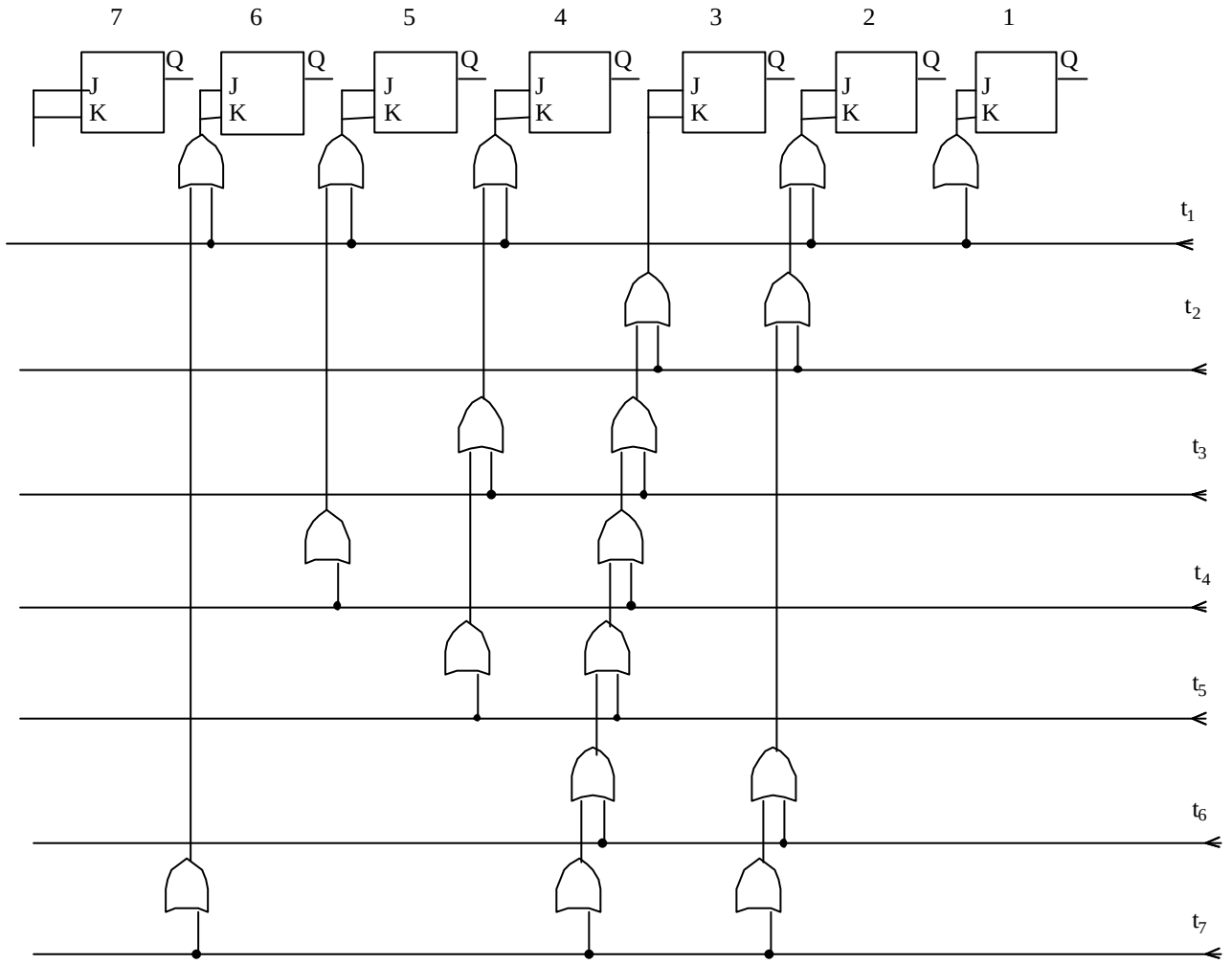

Figure 4

From figure 4 can be deducted that design of a Petri net can be done with an OR network gates connected to 7 J-K latches circuits. Also it can be implemented with a PLA (Programmable Logic Array) circuits.
Initially, the J-K latches must be reset (clear marked point) and then set (set marked point), like in figure 5.

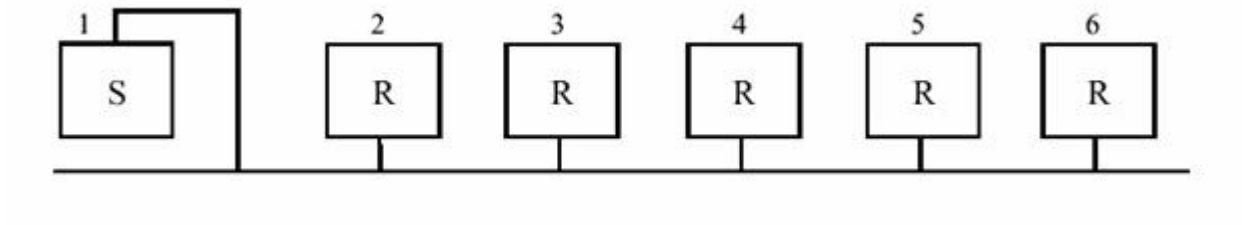

Figure 5

The final implementation of the Petri net system using J-K latches and logic gates is shown on figure 6.
The entire digital system works asynchronous, means that it transit on to another state only if the inputs variables change.

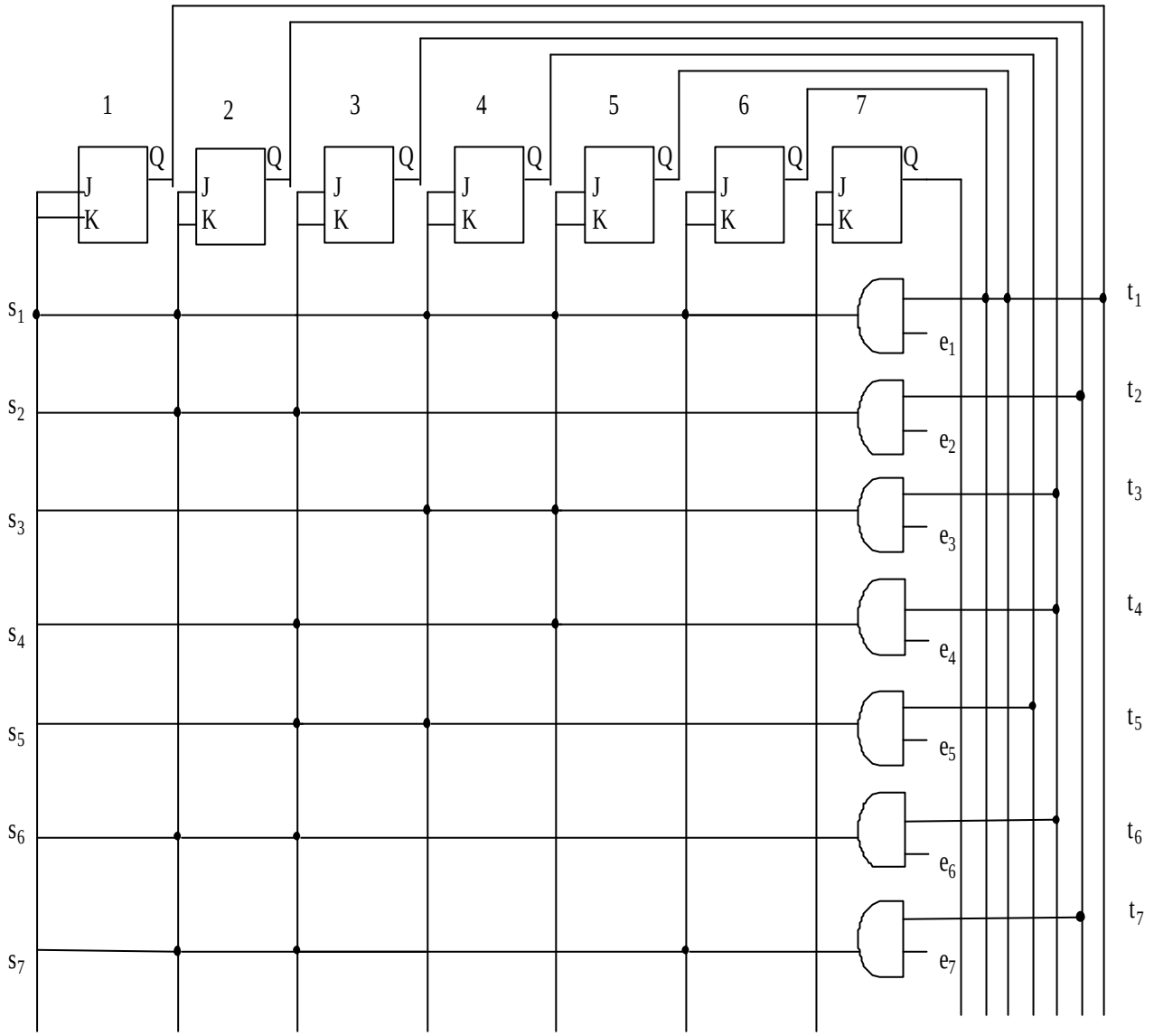

Figure 6

III. CONCLUSIONS

The synthesis method presented on this paper can be successfully applied on systems described with Petri nets graphs, it is a hardware design of the Petri network.
When the system who need to be designed is too much complex, the described method become too hard to implement. In this case, the system must be implemented using state machine algorithm.

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